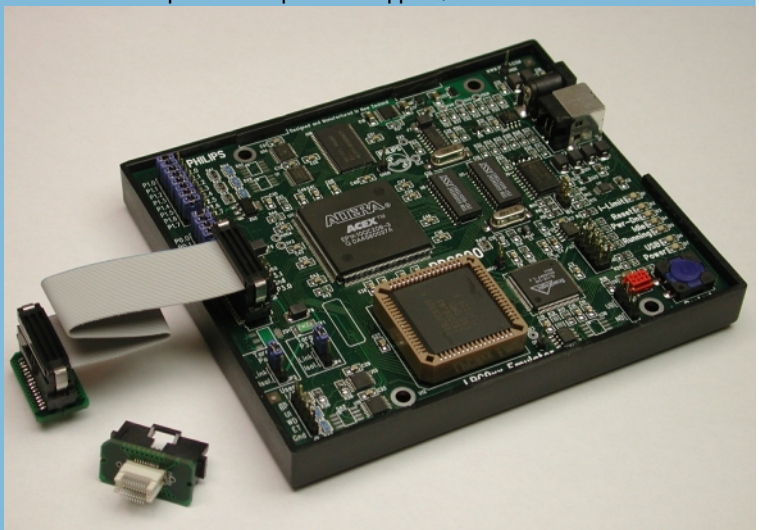
Philips Development System
for P89LPC900 family Microcontrollers

PDS900

Emulator and Programmer

FEATURES

- Emulates and programs Philips P89LPC900 family of high-performance Flash-memory microcontrollers
- Low-cost single-board emulation system with footprint-specific emulation adaptors and device programming adaptor
- Real-time transparent in-circuit emulation to full rated device speed over full device voltage range
- 16k bytes for user program code (full extent of P89LPC900 family address range)
- Real-time trace (112k frames x 32 bits) including 12x user input channels
- Multiple breakpoint sources
- Trigger output for synchronising external test equipment
- Programmable clock source, clock frequency, supply voltage, supply current limit, and digital signal source
- Up to 250mA supply to user target at programmed voltage with programmable current limit
- Fast USB interface to host PC
- Sophisticated Windows-based debugging environment
- Fully soft FPGA logic and system controller firmware
- Free updates and product support, Web-aware



Includes emulation footprint adaptors for TSSOP20, TSSOP28 and PLCC28 packages, and a programming adaptor for PLCC28 packages. Emulation and programming adaptors for other packages available separately.

The PDS900 emulation/programming system may be ordered from Philips Semiconductors or their distributors under part number **PDS900 SD**. For Internet sales, accessories, and support visit **www.pds51.com** or **www.acqura.com**.

DESCRIPTION

The PDS900 is an affordable fully-featured in-circuit emulation system and device programmer for Philips new P89LPC900 family of high-performance microcontrollers.

It allows complete control over execution of a user's program and access to all internal registers and memory spaces of the target microcontroller, without consuming any device resources or introducing other non-standard behaviour, and can program the Flash program memory and configuration data areas of packaged devices.

A P89LPC900 family microcontroller in the user's target system can be replaced with an appropriate footprint adaptor connected via a short flexible ribbon cable to the PDS900 emulator. Program code can then be loaded into the PDS900 and run, and registers and data memory can be examined and modified in order to perform program debugging and optimisation.

The PDS900 has sufficient memory to allow emulation and programming of the full address range of the P89LPC900 family (16k bytes), and recording of a trace history comprising 112k frames of 32-bit data. Trace data is recorded in real time for every machine cycle and comprises address, status, and 12 channels from external inputs. Additional memory provides 16k breakpoints, ancillary control, and output functions.

A PLL-based programmable clock source, and a programmable power supply, allows emulation over the full range of clock frequencies and supply voltages supported by the target microcontroller. The microcontroller can be clocked from this programmable clock source or from the various internal clock sources of the P89LPC900 family devices. For maximum convenience the emulator can supply up to 250mA at the programmed voltage to the user's target system, with a programmable current limit for added protection. An isolated universal mains power supply is included in the box and eliminates potential problems with earth loops.

A trigger output permits synchronisation of an external oscilloscope or logic analyser to any selection of fetch addresses in the 16k address range, and an external digital input can be qualified by any selection of fetch addresses in order to break execution. A continuous clock source with individually-programmable high and low periods is provided to hold off any external watchdog when execution of user code is stopped, or can be used as a basic digital signal source during development.

The PDS900 connects to a host PC via a USB interface that provides ease of installation and fast communication. A sophisticated Windows-based debugging and device programming environment supports all popular code generation tools from 3rd-party vendors.

The PDS900 design is uniquely "soft" in that all software, firmware, and programmable logic can be field-upgraded in order to improve performance or add features. Upgrades are available free of charge from the Web and the debugger can be configured to automatically advise of new updates and download and install them as desired.

Philips Development System for P89LPC900 family Microcontrollers

PDS900

SPECIFICATIONS

Architecture
- Single-board in-circuit emulator
- Footprint specific emulation adaptor
- Programmer with package adaptors
- Fast USB interface to host PC (cable included)
- Windows-based debugger
- Field-upgradeable FPGA logic and control firmware

Emulation
- Transparent (except steals 2 bytes of stack)
- Real-time to beyond rated target device speed
- Full 16k bytes of memory for user programs

Trace Memory
- 112k frames deep, 32 bits wide
- One frame recorded per machine cycle:
  - 14-bit program address
  - Cycle status (instruction fetch, operand fetch, interrupt, idle, etc.)
  - 12x digital user input signal channels

Breakpoints
- 16k on program fetch address (hardware)
- 16k on fetch address and external input
- Break on trace full (112k frames)
- Break after N instructions (N=1..2^{32})
- Break on fetch outside valid program

Trigger Output
- For synchronising external equipment
- 16k trigger points on program fetch address
- 4 modes each (none, pulse-invert, set, clear)

Other Interface Signals
- Watchdog output - to hold off external watchdog resets when execution stopped, or use as basic digital signal source (independently programmable high - low period from 100us to 6s in 100us steps)
- Uncommitted input for future feature
- Optional reset to user's target system

Processor Clock
- From internal device clock sources or external PLL synthesiser with quartz crystal reference
- Synthesiser programmable from 25kHz to 100MHz at better than 0.1% accuracy for any frequency (usable upper freq. limited by target device)
- Optimise for PLL jitter or frequency accuracy
- Processor clock may be optionally routed to target

Processor and System Power Supply
- Programmable from 0 to 3.6V in 25mV steps (usable lower voltage limited by target device)
- Up to 250mA at the programmed voltage can optionally be supplied to target with current limit programmable in 1mA steps
- Supplied with isolated universal mains power supply

Indicators
- System power
- USB communications/system activity
- Microcontroller running (executing user code)
- Microcontroller in idle state
- Microcontroller in power-down state
- Microcontroller in reset state
- Current-limit exceeded

Physical and Environmental
- Board-level product in shielded plastic base
- 130 x 110 x 15mm (excluding adaptors, etc.)
- Complies with European CE specifications

Programming Adaptor
- Parallel mode for maximum functionality
- Detects device presence and correct orientation
- Connects in place of emulation footprint adaptor
- Supported by Windows debugging environment
- PLCC28 socket on-board for low-volume use
- Package adaptors available for higher volume use (PLCC28) and other device packages
- Start button and Pass/Fail LED indicators

WINDOWS DEBUGGING ENVIRONMENT

Requirements
- Pentium-class PC with 128MB RAM, USB Port, Windows 95 (OSR2.5), 98, ME, 2k, or XP

Features
- Supports all popular 8051 code-generation tools
- Source-level debugging with standard OMF files
- Project-based for rapid swapping between projects
- Rich feature set, Borland-compatible key bindings
- Any number of panes displaying any of:
  - C or Assembly-language source
  - Symbolic program code disassembly
  - Mixed source and code disassembly
  - Internal or Auxiliary RAM (AUXRAM)
  - EEROM data array
  - Stack area
  - Trace record
  - Watch (display/modify) any SFR or variable in any supported format:
    - binary, octal, hex, unsigned, signed, float, ASCII character, Pascal or C string (numerical values from 1..4 bytes, big- or little-endian)

Emulation Controls (representative subset)
- Reset target
- Set execution point (PC)
- Run/Stop
- Run until instruction at cursor
- Step/Step N times
- Step into procedure/function
- Step over procedure/function
- Leave (run until procedure/function exits)
- Follow (reposition view at destination of instruction)
- Clear trace buffer
- Run until trace buffer full or filled again
- Program/verify device Flash program array
- Program/verify device configuration data

Trace Display
- 112k lines (frames)
- Address, Status, 12x digital user inputs
- Disassembly of executed instruction
- Special cycles (eg INTACK) highlighted
- Position to corresponding code in source

On-line Help
- Context-sensitive
- Full P89LPC900 family (8xC51) instruction reference

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